INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY HIGH POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit of the following provisional patent applications, which are hereby incorporated by reference herein.

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000;

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by Joseph T. DiBene II, David H. Hartke, and James M. Broder, filed February 6, 2001;

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 16, 2001;

Application Serial No. 60/292,125, entitled "VORTEX HEATSINK FOR LOW PRESSURE DROP HIGH PERFORMANCE THERMAL MANAGEMENT ELECTRONIC ASSEMBLY SOLUTIONS," by Joseph T. DiBene II, Farhad Raiszadeh, filed May 18, 2001;

Application Serial No. 60/299,573, entitled "IMPROVED MICRO-I-PAK STACK-UP ARCHITECTURE," by Joseph T. DiBene, Carl E. Hoge, and David H. Hartke, filed June 19, 2001;

Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 27, 2001;

Application Serial No. 60/304,929, entitled " BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001;

Application Serial No. 60/304,930, entitled "MICRO-I-PAK," by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001;

Application Serial No. 60/310,038, entitled "TOOL-LESS CONCEPTS FOR BORREGO," by Edward J. Derian and Joseph T. DiBene II, filed August 3, 2001;

Application Serial No. 60/313,338, entitled "TOOL-LESS PRISM IPA ASSEMBLY TO SUPPORT IA64 MCKINLEY MICROPROCESSOR," by David H. Hartke and Edward J. Derian, filed August 17, 2001; and

Application Serial No. --/---,---, entitled "MICRO-SPRING CONFIGURATIONS FOR POWER DELIVERY FROM VOLTAGE REGULATOR MODULES TO INTEGRATED CIRCUITS AND MICROPROCESSORS," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed November 8, 2001.

This patent application is also continuation-in-part of the following co-pending and commonly assigned patent applications, each of which applications are hereby incorporated by reference herein:

Application Serial No. 09/885,780, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed June 19, 2001, which is a continuation of application Serial No. 09/353,428, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by Joseph T. DiBene II and David H. Hartke, filed July 15, 1999 and now issued as U.S. Patent No. 6,304,450;

Application Serial No. 09/432,878, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING FOR POWER DELIVERY," by Joseph T. DiBene II and David H. Hartke, filed November 2, 1999;

Application Serial No. 09/727,016, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY" by Joseph T. DiBene II and David Hartke, filed November 28, 2000, which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/167,792, entitled "EMI CONTAINMENT USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed November 29, 1999;

Application Serial No. 60/171,065, entitled "INTER-CIRCUIT ENCAPSULATION PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed December 16, 1999;

Application Serial No. 60/183,474, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED

PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGHS AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled 'HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled 'HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000; and

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000,

Application Serial No. 09/785,892, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II, David H. Hartke, James J. Hjerpe Kaskade, and Carl E. Hoge, filed February 16, 2001 which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/183,474, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT, by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

Application Serial No. 60/186,769, entitled "THERMACEP SPRING BEAM," by Joseph T. DiBene II and David H. Hartke, filed March 3, 2000;

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled 'EMI FRAME WITH POWER FEED-THR0UGHS AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled 'HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY HIGH POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING,." By Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, James M. Broder, and Joseph S. Riel, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by David H. Hartke, James M. Broder, and Joseph T. DiBene II, filed February 6, 2001,

Application Serial No. 09/798,541, entitled "THERMAL/MECHANICAL SPRINGBEAM MECHANISM FOR HEAT TRANSFER FROM HEAT SOURCE TO HEAT DISSIPATING DEVICE," by Joseph T. DiBene II, David H. Hartke, Wendell C. Johnson, and Edward J. Derian, filed March 2, 2001 which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 06/185,769, entitled "THERMACEP SPRING BEAM," by Joseph T. DiBene II and David H. Hartke, filed March 3, 2000;

Application Serial No. 60/183,474, entitled "METHOD AND APPARATUS FOR PROVIDING POWER TO A MICROPROCESSOR WITH INTEGRATED THERMAL AND EMI MANAGEMENT," by Joseph T. DiBene II and David H. Hartke, filed February 18, 2000;

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGHS AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial N. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by David H. Hartke, James M. Broder, and Joseph T. DiBene II, filed February 6, 2001,

Application Serial No. 09/801,437, entitled "METHOD AND APPARATUS FOR DELIVERING POWER TO HIGH PERFORMANCE ELECTRONIC

ASSEMBLIES" by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, James M. Broder, Edward J. Derian, Joseph S. Riel, and Jose B. San Andres, filed March 8, 2001, which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGHS AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT, by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND

SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE" by David H. Hartke, James M. Broder and Joseph T. DiBene II, filed February 6, 2001,

Application Serial No. 09/802,329, entitled "METHOD AND APPARATUS FOR THERMAL AND MECHANICAL MANAGEMENT OF A POWER REGULATOR MODULE AND MICROPROCESSOR IN CONTACT WITH A THERMALLY CONDUCTING PLATE" by Joseph T. DiBene II and David H. Hartke, filed March 8, 2001 which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/187,777, entitled "NEXT GENERATION PACKAGING FOR EMI CONTAINMENT, POWER DELIVERY, AND THERMAL DISSIPATION USING INTER-CIRCUIT ENCAPSULATED PACKAGING TECHNOLOGY," by Joseph T. DiBene II and David H. Hartke, filed March 8, 2000;

Application Serial No. 60/196,059, entitled "EMI FRAME WITH POWER FEED-THROUGHS AND THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT, by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000; and

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE" by David H. Hartke, James M. Broder and Joseph T. DiBene II, filed February 6, 2001,

Application Serial No. 09/910,524, entitled "HIGH PERFORMANCE THERMAL/MECHANICAL INTERFACE FOR FIXED-GAP REFERENCES FOR HIGH HEAT FLUX AND POWER SEMICONDUCTOR APPLICATIONS", by Joseph T. DiBene, II, David H. Hartke, Wendell C. Johnson, Farhad Raiszadeh, Edward J. Darien and Jose B. San Andres, filed July 20, 2001 which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/219,506, entitled "HIGH PERFORMANCE THERMAL/MECHANICAL INTERFACE," by Joseph T. DiBene II, David H. Hartke, and Wendell C. Johnson, filed July 20, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene Ii and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000;

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE," by Joseph T. DiBene II, David H. Hartke, and James M. Broder, filed February 6, 2001;

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 16, 2001;

Application Serial No. 60/292,125, entitled "VORTEX HEATSINK FOR LOW PRESSURE DROP HIGH PERFORMANCE THERMAL MANAGEMENT ELECTRONIC ASSEMBLY SOLUTIONS," by Joseph T. DiBene II and Farhad Raiszadeh, Filed May 18, 2001;

Application Serial No. 60/299,573, entitled "IMPROVED MICRO-I-PAK STACK-UP ARCHITECTURE," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 19, 2001;

Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 27, 2001;

Application Serial No. 60/304,929, entitled "BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001; and

Application Serial No. 60/304,930, entitled "MICRO-I-PAK, by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001,

Application Serial No. 09/921,153 entitled "VAPOR CHAMBER WITH INTEGRATED PIN ARRAY", by Joseph T. DiBene, II and Farhad Raiszadeh, filed on August 2, 2001 which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No., 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000;

Application Serial No. 60/266,941, entitled "MECHANICAL INTERCONNECTION TECHNOLOGIES USING FLEX CABLE INTERCONNECT FOR POWER DELIVERY IN 'INCEP' INTEGRATED ARCHITECTURE" by David H. Hartke, James M. Broder and Joseph T. DiBene II, filed February 6, 2001;

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 16, 2001;

Application Serial No. 60/292,125, entitled "VORTEX HEATSINK FOR LOW PRESSURE DROP HIGH PERFORMANCE THERMAL MANAGEMENT ELECTRONIC ASSEMBLY SOLUTIONS," by Joseph T. DiBene II and Farhad Raiszadeh, Filed May 18, 2001;

Application Serial No. 60/299,573, entitled "IMPROVED MICRO-I-PAK STACK-UP ARCHITECTURE," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 19, 2001;

Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 27, 2001;

Application Serial No. 60/304,929, entitled "BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001; and

Application Serial No. 60/304,930, entitled "MICRO-I-PAK, by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001,

Application Serial No. 09/818,173, entitled "INTER-CIRCUIT ENCAPSULATED PACKAGING," by David H. Hartke and Joseph T. DiBene II, filed March 26, 2001, which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/196,059, entitled "THERMAL INTERFACE MATERIAL IN AN AGGREGATE DIAMOND MIXTURE," by Joseph T. DiBene II and David H. Hartke, filed April 10, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

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ARCHITECTURE" by David H. Hartke, James M. Broder and Joseph T. DiBene II, filed February 6, 2001;

Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

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Application Serial No. 60/301,753, entitled "INTEGRATED POWER DELIVERY USING HIGH PERFORMANCE LINEAR REGULATORS ON PACKAGE WITH A MICROPROCESSOR," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 27, 2001;

Application Serial No. 60/304,929, entitled "BORREGO ARCHITECTURE," by David H. Hartke and Joseph T. DiBene II, filed July 11, 2001; and

Application Serial No. 60/304,930, entitled "MICRO-I-PAK, by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001,

Application Serial No. 09/921,152, entitled "HIGH SPEED AND DENSITY CIRCULAR CONNECTOR FOR BOARD-TO-BOARD INTERCONNECTION SYSTEMS," by David H. Hartke and Joseph T. DiBene II, filed on August 2, 2001;

Application Serial No., 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/222,407, entitled "VAPOR HEATSINK COMBINATION FOR HIGH EFFICIENCY THERMAL MANAGEMENT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

Application Serial No. 60/219,813, entitled "HIGH CURRENT MICROPROCESSOR POWER DELIVERY SYSTEMS," by Joseph T. DiBene II, filed July 21, 2000;

Application Serial No. 60/232,971, entitled "INTEGRATED POWER DISTRIBUTION AND SEMICONDUCTOR PACKAGE," by Joseph T. DiBene II and James J. Hjerpe, filed September 14, 2000;

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Application Serial No. 09/921,153, entitled "VAPOR CHAMBER WITH INTEGRATED PIN ARRAY," by Joseph T. DiBene II, and Farhad Raiszadeh, filed August 2, 2001, which claims priority to the following U.S. Provisional Patent Applications:

Application Serial No. 60/222,386, entitled "HIGH DENSITY CIRCULAR 'PIN' CONNECTOR FOR HIGH SPEED SIGNAL INTERCONNECT," by David H. Hartke and Joseph T. DiBene II, filed August 2, 2000;

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Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

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Application Serial No. 60/299,573, entitled "IMPROVED MICRO-I-PAK STACK-UP ARCHITECTURE," by Joseph T. DiBene II, Carl E. Hoge, and David H. Hartke, filed June 19, 2001;

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Application Serial No. 60/304,930, entitled "MICRO-I-PAK, by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001, and

Application Serial No. --/---,---, entitled "ULTRA-LOW IMPEDANCE POWER INTERCONNECTION SYSTEM FOR ELECTRONIC PACKAGING," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed October 30, 2001, which application claims priority to the following U.S. Provisional Applications:

Application Serial No. 60/251,222, entitled "INTEGRATED POWER DELIVERY WITH FLEX CIRCUIT INTERCONNECTION FOR HIGH DENSITY POWER CIRCUITS FOR INTEGRATED CIRCUITS AND SYSTEMS," by Joseph T. DiBene II and David H. Hartke, filed December 4, 2000;

Application Serial No. 60/251,223, entitled "MICRO-I-PAK FOR POWER DELIVERY TO MICROELECTRONICS," by Joseph T. DiBene II and Carl E. Hoge, filed December 4, 2000;

Application Serial No. 60/251,184, entitled "MICROPROCESSOR INTEGRATED PACKAGING," by Joseph T. DiBene II, filed December 4, 2000;

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Application Serial No. 60/277,369, entitled "THERMAL-MECHANICAL MEASUREMENT AND ANALYSIS OF ADVANCED THERMAL INTERFACE MATERIAL CONSTRUCTION," by Joseph T. DiBene II, David H. Hartke and Farhad Raiszadeh, filed March 19, 2001;

Application Serial No. 60/287,860, entitled "POWER TRANSMISSION DEVICE," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 1, 2001;

Application Serial No. 60/291,749, entitled "MICRO I-PAK ARCHITECTURE HAVING A FLEXIBLE CONNECTOR BETWEEN A VOLTAGE REGULATION MODULE AND SUBSTRATE," by Joseph T. DiBene II, filed May 16, 2001;

Application Serial No. 60/291,772, entitled "I-PAK ARCHITECTURE POWERING MULTIPLE DEVICES," by Joseph T. DiBene II, David H. Hartke, Carl E. Hoge, and Edward J. Derian, filed May 16, 2001;

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Application Serial No. 60/304,930, entitled "MICRO-I-PAK," by Joseph T. DiBene II, Carl E. Hoge, David H. Hartke, and Edward J. Derian, filed July 11, 2001;

Application Serial No. 60/310,038, entitled "TOOL-LESS CONCEPTS FOR BORREGO," by Edward J. Derian and Joseph T. DiBene II, filed August 3, 2001; and

Application Serial No. 60/313,338, entitled "TOOL-LESS PRISM IPA ASSEMBLY TO SUPPORT IA64 MCKINLEY MICROPROCESSOR," by David H. Hartke and Edward J. Derian, filed August 17, 2001.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to systems and methods for electrically interconnecting circuit boards, and in particular to a system and method for transmitting high power through a flexible circuit interconnect from the edge of a printed circuit board, through multiple coaxial interconnects, to a power regulator board, all within a reduced form factor.

2. Description of the Related Art

As processing speeds continue to increase, the power demands of the processors used in such systems (such as microprocessors for servers and desktop systems) have increased dramatically. While patent applications referenced above have shown that it is desirable to mount power conversion modules (which convert higher voltage signals to low voltage-high current power signals) close to the devices that have high power dissipation requirements, it is often difficult to do so due to thermal, mechanical and other constraints.

One reason for this difficulty is that the power in such devices often requires large heatsinks which encroach on the power conversion modules and forces the power conversion to be further away then desired. Thus, what often results is a fairly high dynamic voltage drop across the interconnection of the power interconnect, due to high slew-rate switching of the load, typically resulting in false switching of the device itself which may corrupt data. Therefore, it is seen that there is a need to bring both the power regulation closer to the load while maintaining a low impedance, small form factor, and easy to assemble construction which is of reasonably low cost. The present invention satisfies that need.

SUMMARY OF THE INVENTION

To address the requirements described above, the present invention discloses a method and apparatus for electrically interconnecting a first circuit board having a power conditioning circuit and a second circuit board having a power dissipating component disposed therebelow along a z (vertical) axis. In an illustrative embodiment, the apparatus comprises a first flexible circuit having a first set of raised conductive contacts, the first flexible circuit disposed on a first side of the second circuit board; and a second flexible circuit having a second set of raised conductive contacts, the second flexible circuit disposed on a second side of the second circuit board opposing the first side of the second circuit board. A power signal from the power conditioning circuit is provided to the second circuit board at least in part by either the first set of raised conductive contacts

on the first flexible circuit or the second set of raised conductive contacts on the second flexible circuit. Further, a ground return is provided to the second circuit board by the set of raised conductive contacts that are not used to provide the power signal from the power conditioning circuit to the second circuit board.

The present invention therefore can be described by a power interconnecting structure between a power regulator board and the card edge connector of an interposer board which houses a high performance microprocessor using a low impedance, low cost, flexible circuit. The housing may be made of molded plastic and the flexible circuits may be single-sided. The flexible circuit has multiple coaxial interconnects which interconnect to a power regulator module mounted directly above the edge-card interface of the interposer or the flexible circuit can connect directly to the power module without the intervention of the coaxial interconnects. A substrate may be mounted between or on the flexible circuits for interconnect to the coaxial connectors or the connection may be made directly to the flexible circuits themselves. The coaxial interconnects can be disconnectable at the flexible circuit side or the power module interface or may be permanently attached to both sides. Pressure to the edge card contact region on the interposer is maintained through either an elastomeric pad residing within the housing or through spring fingers located in the same area as the elastomer which maintains a constant force for a high conductivity electrical connection by pressing against the back of the flexible circuit opposite the side the bumps are located. Low electrical impedance is maintained by keeping the separation between the flexible circuits very small throughout the design. The electrical connection between the power regulator module and interposer requires very little space and maintains a very low electrical impedance while compacting the overall construction by placing the integrated power regulator module above the interposer itself. The unit also is designed where the flexible circuits compensate for mechanical tolerances in the stackup relieving forces from being applied to the interposer and its associated thermal interface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a diagram illustrating a section view of the power interconnecting structure wherein the flexible circuit is split into separate circuits using a rigid circuit board which connect to the card edge connection pads of an interposer and, through coaxial interconnects attached to the rigid circuit board, join to a power regulator module;

FIG. 1B is a diagram illustrating a plan section view of the embodiment in FIG. 1A;

FIG. 2A is a diagram showing a section view where a single flexible circuit is used rather than two and the flexible circuit wraps around internal to the housing embracing the card edge connection pads of an interposer and, through coaxial interconnects, join to a power regulator module;

FIG. 2B is a diagram illustrating a plan section view of the embodiment in FIG. 2A;

FIG. 3 illustrates a section view of the power interconnecting structure where the flexible circuits embrace the interposer board and are directly attached to coaxial interconnects that are permanently attached to a power regulator module;

FIG. 4A is diagram illustrating a section view of the power interconnecting structure where the flexible circuit attaches directly to the power regulator module without use of a coaxial interconnect;

FIG. 4B is a diagram showing a plan view of the power interconnecting structure where the flexible circuit attaches directly to the power regulator module without use of a coaxial interconnect; and

FIGs. 5A and 5B are diagrams showing further detail regarding the flexible circuits.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following description, reference is made to the accompanying drawings which form a part hereof, and which is shown, by way of illustration, several embodiments of the present invention. It is understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

FIG. 1A and 1B are diagrams illustrating a power interconnecting structure 10. Using the illustrated power interface assembly 11, the power interconnecting structure 10 provides power (e.g. a power signal) between a first circuit board 101 having a power conditioning/regulating circuit represented by module 208 and a second circuit board such as a processor interposer board 120 which houses a high performance microprocessor 210. Processor interposer board 120 utilizes a first set of continuous strip edge card contact pads 121 and 122 to receive power from power interface assembly 11.

Arbitrarily, pad 121 is generally assigned ground potential and pad 122 is assigned power. A first (upper) flexible circuit 116 is provided with either a continuous raised strip or a set of individual raised bump contacts 117 which electrically engage with the pad 121 on interposer 120. The strip 117 or individual contact bumps can be formed as a part of the flexible circuit 116 using either electro-plating methods or formed and solder joined contacts as currently practiced in the industry. In a similar manner, a lower flexible circuit 115 is also provided with a continuous raised strip 117 or individual contact bumps. In the illustrated embodiment, each flexible circuit 116, 117 carries only one polarity of power, e.g., ground or power.

Pressure is applied to the contact area (the junction between interposer pad 121 and strip/contact 117) utilizing compressible members 118 such as elastomeric pads residing in a cavity 202 formed by the upper housing 112 and the lower housing 113. Although shown as an elastomeric pad it is also possible to utilize a spring finger strip which can be located in the same area as the elastomeric pad 118 to provide a uniform pressure to the contact area. Upper flexible circuit 116 and lower flexible circuit 115 are

joined to rigid circuit board 111 which provides a mounting structure for coaxial interconnects 110 and serves as a limit stop when inserting power interface assembly 11 into processor interposer 120.

In the illustrated embodiment, one or more coaxial interconnects 110 are permanently attached to circuit board 111 and a separable connection is provided at power regulator module 101 utilizing screw 102 and washer 103 which provide a high pressure contact between the outer cylinder 110A of the coaxial interconnect 110 and ground pads 204 on power regulator module 101. The power conditioning circuitry 208 is then electrically connected to the ground pads 204 by a combination of vias and/or conductive planes and/or traces in the first circuit board 101.

Similarly, the power circuit through the center conductor 110B of coaxial connector 110 is passed through the screw 102 and washer 103 to power polarity pads 212 on the top of the first circuit board 101. The power conditioning circuitry 208 is then electrically connected to the power pads 212 by a combination of vias and/or conductive planes and/or traces in the first circuit board 101.

It should be noted that other designs of coaxial interconnect are possible and are disclosed in patents referenced above and hereby incorporated by reference herein.

The ends of flexible circuits 116, 115 are wrapped around the ends of the first housing 112 and the second housing 113 and are secured in place using attachment 114 which can preferably take the form of a heat stake if housings 112, 113 are plastic or may utilize riveting methods if housings 112, 113 are formed of metal. Fasteners 123 secure the upper housing 112 to the lower housing 113 while "trapping in place" rigid circuit board 111, thus creating a single assembly 11 in which the second circuit board 120 can be inserted and which can be secured to the first circuit board 101 using disconnectable fasteners, such as the screw 102 and washer 103.

Although the mechanical tolerances of the stackup between the first circuit board 101 and the second circuit board 120 in the z-axis (vertical) direction are small, such tolerances must be accounted for, thus requiring some degree of flexibility between these

components. Flexible circuits 115 and 116 provide for this mechanical acceptance in the area between the contact pad 117 and the rigid board 111.

The interconnect structure shown in FIGs. 1A and 1B provide an electrical connection between the first circuit board 101 and the second circuit board 120 having very low electrical interconnect impedance. The inductive portion of this impedance is kept low by minimizing the loop area between contact pads 117 and coaxial interconnect 110 attachment and by using the coaxial interconnects 110 which also have very low inductance.

FIGs. 2A and 2B are diagrams illustrating a power interconnect structure 10 similar to that described in FIGs. 1A and 1B but which utilize a single contiguous flexible circuit 123 having a first flexible circuit portion 123A and a second flexible circuit portion 124B enclosed in power interface assembly 12. In this embodiment, flexible circuits 123A and 123B may be two separate circuits that are joined in the area of coaxial interconnect 110 forming a single assembly. As shown, the second flexible circuit portion 123B wraps around internally in upper housing 125 and lower housing 126 and coming in contact with the lower pad 122 on the second circuit board 120. Electrical connectivity is made between a conductive surface on the flexible circuit 123B (such as the contact bumps described above with respect to FIGs. 1A and 1B) and the lower pad 122.

Bosses 128 which may be formed as a part of upper and lower housings 125 and 126 serve to hold in place flexible circuit ends 123A and 123B. This can be accomplished, for example, by using bosses 128 with surface features extending towards the flexible circuit 123, cooperatively interfacing with matching features such as holes extending vertically through flexible circuit 123. In addition, bosses 128 serve as limit stops when inserting power interface assembly 11 into second circuit board 120. Fasteners 127 secure the upper housing 125 to the lower housing 126.

FIG. 3 is a diagram illustrating a power interconnect structure 10 similar to that described in FIG. 1A and 1B in which the power interface assembly 13 permits the coaxial interconnects 110 to be permanently attached to the first circuit board 101 in an

inverted arrangement. Upper flexible circuit 130A and lower flexible circuit 130B come together in yoke area 132 and are in intimate surface contact with one another over the area where coaxial interconnect 110 interfaces to the two flexible circuits. Insulating material may be placed between the flexible circuits in this area to avoid the two power circuits from shorting one another, if necessary. Bosses 128 which can be a part of upper and lower housings 112 and 113 serve to hold in place flexible circuits 131 and 132, as described above with respect to FIGs. 2A and 2B. An advantage of this arrangement is the reduction in loop area between contact pads 117 and coaxial interconnect 110. A secondary advantage is the simplification of the flexible circuit structure eliminating the need for rigid board 111.

FIGs. 4A and 4B are diagrams illustrating a further embodiment of the power interconnect structure 10. Here, flexible circuits 142 and 143 are formed in a manner similar to that which was described with respect to FIG. 3, wherein a yoke area 132 is used to bring the upper flexible circuit 143 in contact with the lower flexible circuit 142. Unlike the embodiment in FIG. 3, however, after which the two flexible circuits 142, 143 are joined, they egress through a rear aperture formed by the upper housing 140 and lower housing 141. The upper 140 and lower 141 housings can either entrap the flexible circuits 142 and 143 using surface features or friction, or mold them in place forming one overall assembly 13.

After the flexible circuits 142 and 143 egress the housings 140 and 141 they are brought up to the first circuit board 101 where the ends of each flexible circuit are interdigitated forming alternating soldered connection tabs 146 and 146 which are soldered to corresponding alternating power and ground surface pads 144 and 145 on the lower surface of the first circuit board 101. This arrangement provides a low inductance connection due to the small loop area between the interdigitated connections comprising of pads 144 and 145, and simplifies solder assembly, since a simple bar solder operation on one side of the flexible circuits can be used to solder all of the tabs of the flexible circuits to the pads on the power regulator module 101.

FIGs. 5A and 5B are diagrams showing further detail regarding the flexible circuits 115, 116. FIG. 5A is a diagram looking up from the bottom into first flexible circuit 115. The outline shown for flexible circuit 115 defines the perimeter of the copper foil of said flexible circuit pattern which forms the power interconnection. It will be understood that said flexible circuit further consists of additional insulating cover sheets in selected areas. Holes 504 are used for inserting attachments 114 through flexible circuit 115 thereby securing flexible circuit to housing 113. Plated through holes 508 terminate in isolated pad 510 which accommodates the solder connection of outer cylinder 110A to second flexible circuit 116. Hole 514 which may be either plated or unplated receives inner cylinder 110B and is soldered to foil surface of flexible circuit 115. Raised bump contacts 117 are shown as a dashed outline and are located on the far side of flexible circuit 115. Dashed line 502 locates the terminus of rigid board 111 to which flexible circuit 115 is laminated.

FIG 5B is a diagram looking down from the top into second flexible circuit 116. Again, the outline shown for flexible circuit 116 defines the perimeter of the copper foil of said flexible circuit pattern which forms the ground interconnection. Hole 516, which receives the inner cylinder 110B, is isolated from the conductive foil of flexible circuit 116 by isolation area 518. Again, raised bump contacts 117 are shown as a dashed outline and are located on the far side of flexible circuit 116.

Those skilled in the art will recognize many modifications may be made to this configuration without departing from the scope of the present invention. For example, part of the power interconnecting structure could be used to provide signals as well as power, from the first circuit board (or an alternate circuit board) to the second circuit board.

Conclusion

This concludes the description of the preferred embodiments of the present invention. The foregoing description of the preferred embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be

exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto. The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.